2189



Attorney's Docket No.: 10559-365001 / P10171
Assignee: Intel Corporation

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Patrick L. Connor et al. Art Unit : 2189
Serial No. : 09/752,099 Examiner : Huynh, Kim T.
Filed : December 28, 2000
Title : A METHOD OF REAL TIME STATISTICAL COLLECTION FOR I/O CONTROLLERS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



REPLY TO ACTION OF JULY 1, 2003

In reply to the Office Action of July 1, 2003, Applicant submits the following remarks.

The applicant appreciates the examiner's thorough examination of the subject application and requests reexamination and reconsideration of the subject application in view of the following remarks.

Concerning item 1 of the subject action, the examiner rejects claims 1-30 under 35 USC §102(e) based on the teachings of Kuo et al (U.S. Patent No.: 6,047,001).

Applicant claims in claim 1:

> a method comprising: (a) receiving status information concerning a size and location of a data packet; (b) receiving statistical information concerning a bus condition; and (c) storing the status information and the statistical information on a storage device using a single write procedure.

Applicant respectfully asserts that Kuo is not a proper basis for a 35 USC §102(e) rejection, as it does not teach each and every element of the applicant's claimed invention. Specifically, Kuo does not disclose elements (b) or (c).

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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In element (b) of applicant's claim 1, applicant claims "receiving statistical information concerning a bus condition". Concerning this "statistical information", the applicant's specifications discloses that:

> A statistics information process 30 receives statistical information 32 from bus 10 concerning various bus conditions (e.g., late collisions, excess collisions, dropped frames... *See applicant's specification, page 2, line 26 - page 3, line 3.*

Applicant respectfully asserts that Kuo fails to disclose a system that processes "statistical information... ...concerning various bus conditions...". Concerning the rejection of element (b) of applicant's claim 1, the examiner relies of Kuo, col. 7, lines 37-65 for support. This passage discloses that:

> FIG. 4 is a block diagram illustrating the write controller 22a for generating frame track information and status information for a transmit data frame written to the transmit buffer (TX.sub.-- SRAM) 18b according to an embodiment of the present invention. As shown in FIG. 4, the write controller 22a is configured for writing a data unit 64, having a data frame 68 and corresponding tracking information 66, into the random access memory 18b. As described below, the memory controller 22a is configured for generating the tracking information including the frame track 66 and the control field 70 based on transfer status signals from either the slave interface 16a or the descriptor management block 24. The write controller 22a includes an address state machine 80, frame information generation logic 82, and byte packing logic 85 for controlling a holding register 86. The byte packing logic 84 is configured for shifting a byte alignment of a data frame received from the BIU 16 prior to storage in the transmit buffer 18b. Specifically, PCI bus transfers may include invalid data bytes at the beginning of a bus transfer indicated by the control/byte enable signal on the PCI bus 12. The byte packing logic 84 performs byte alignment in the holding register 86 to ensure that the first valid data byte in a PCI bus transfer is stored as the first byte in the stored data unit 64 at location D0. The byte packing logic 84 also monitors the number of bytes that have been stored in the transmit SRAM 18b and outputs the byte count for the number of bytes stored in the TX.sub.-- SRAM 18b for the current data frame (saved.sub.-- XB.sub.-- BCNT) to the frame information generation logic 82.

The above passage describes "track information" and "status information", and it appears that the examiner is asserting that Kuo's "status information" is synonymous with the applicant's "statistical information" which, as stated above, concerns "various bus conditions".

Applicant respectfully asserts that the examiner's reliance on the passage within Kuo is improper.

Concerning the status information referenced in the above passage, Kuo discloses that:

> the stored data frame 68 is stored in 32-bit memory locations in a contiguous sequence. The data unit 64 also includes a 32-bit control word 70 storing status information in a memory location contiguous with and following the stored frame data 68. *See Kuo, column 6, lines 53-57, emphasis added.*

Concerning "control word 70", Kuo discloses that:

> the memory controller (XB.sub.-- MMU) 22a stores in the TX.sub.-- SRAM 18b frame track information 66, and status information related to the transmit data frame 68 in a control field 70. *See Kuo, column 6, lines 63-66.*

Accordingly, "control word 70" includes "frame track information" and "status information".

Concerning the frame track information, Kuo discloses that:

> The frame track field 66 is used by the XM.sub.-- MMU 22b to keep track of the location of the corresponding data frame 68 and the TX.sub.-- SRAM 18b. Hence, the frame track 66 enables the XM.sub.-- MMU 22b to quickly flush a stored data unit 63 having transmit frame data 68 and jump to the beginning of the next stored data unit (e.g., 64.sub.2), based on an end of frame address field (ENF ADDR), a count (CNT) field specifying the number of DWORDS (D0, D1, . . . , DLAST), and information in the control field 70. *See Kuo, column 6, lines 66-column 7, line7.*

And concerning the "status information", Kuo claims a step including:

> generating status information specifying conditions of the written data frame following the data frame writing step; and storing the generated status information in a first contiguous memory location following the written data frame. *See Kuo, claim 2.*

Accordingly, the "status information" that Kuo discloses and claims concerns "specifying conditions of the written data frame following the data frame writing step" (as disclosed by Kuo) and, accordingly, does not concern "various bus conditions" (as disclosed and claimed by the applicant).

Accordingly, applicant respectfully asserts that the "status information" disclosed and claimed in Kuo is not equivalent to the "statistical information" disclosed and claimed by the applicant. Therefore, the applicant respectfully asserts that Kuo does not disclose element (b) of applicant's claim 1 and, therefore, Kuo is not a proper basis for a 35 USC §102(e) rejection, as it does not disclose each and every element of the applicant's claimed invention.

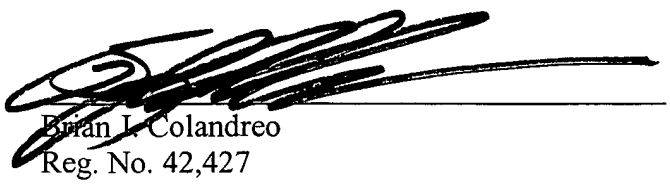
Further, as Kuo does not disclose the storage of "statistical information" (as described in the applicant's specification), Kuo clearly cannot disclose element (c) of applicant's claimed invention, namely "storing the status information and the statistical information on a storage device using a single write procedure". *Emphasis added.*

Accordingly applicant respectfully asserts that applicant's claim 1 is patentable of the cited reference. Further, applicant respectfully asserts that claims 2-9 are also patentable, as they depend (either directly or indirectly) on a patentable base claim. Additionally, as independent claims 10, 26, and 28 each reference "statistical information", applicant respectfully asserts that these claims are also patentable over the cited reference. Further, as dependant claims 1125, 27, and 29-30 each depend (either directly or indirectly) upon an allowable base claim, applicant respectfully asserts that these claims are also patentable.

Applicant asks that all claims be allowed. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: August 8, 2003



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